AMENDMENTS TO THE CLAIMS

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Currently Amended) A phase locked loop (PLL) circuit ~~(1) at least including~~ comprising:

a loop input ~~(11)~~;

a phase detector section ~~(2,3)~~ for detecting a phase difference between an input signal and a reference signal, said phase detector section ~~(2,3)~~ having a detector input connected to said loop input, a reference input and a detector output for outputting a signal related to said phase difference;

a controlled oscillator ~~(4)~~ having an input communicatively connected to said detector output and an oscillator output connected to a loop output ~~(12)~~; and

a feedback circuit~~(13)~~ connecting said oscillator output to said reference input,

wherein

said feedback circuit includes a device ~~(7 ;71-74)~~ having a transfer function with at least one zero, and the phase locked loop circuit ~~(1)~~ has a closed loop transfer function without zeros.

2. (Currently Amended) A phase locked loop circuit as claimed in claim 1, further ~~including~~ comprising a filter section ~~(4)~~ having a filter input connected to said detector output and a filter output connected to said oscillator input.

3. (Currently Amended) A phase locked loop circuit as claimed in claim 1 ~~claims 1 or 2~~, wherein said feedback circuit further includes at least one frequency divider device ~~(6; 7; 72; 73)~~.

4. (Currently Amended) A phase locked loop circuit as claimed in claim 3, wherein said frequency divider device is connected to a delta-sigma modulator device ~~(8)~~.

5. (Currently Amended) A phase locked loop circuit as claimed in claim 3 ~~claim 3 or 4~~, wherein said frequency divider device ~~(6; 7; 72;)~~ has a transfer function with said zero.

6. (Currently Amended) A phase locked loop circuit as claimed in claim 3 ~~any one of claims 3-5~~, wherein said feedback circuit includes a first frequency divider device ~~(6)~~ and a second frequency divider device ~~(7; 72; 73)~~, said second frequency divider device having a transfer function with a zero.

7. (Currently Amended) A phase locked loop circuit as claimed in claim 6, wherein said first frequency divider device ~~(6)~~ and said second frequency divider device ~~(7;72;73)~~ are connected in parallel and wherein an output of the first frequency divider device and an output of the second frequency divider device are each connected to an input of a second combiner device ~~(200)~~, and wherein an output of the second combiner device is connected to the reference input of the phase detector section ~~(2,3)~~.

8. (Currently Amended) A phase locked loop circuit as claimed in claim 6, wherein an output of the second frequency divider device ~~(73)~~ is connected to an first input of a second combiner device ~~(210)~~, a second input of the second combiner device is connected to the output of the phase detector, an output of the second combiner device is communicatively connected to the VCO, and wherein:

the second divider device comprises a phase detector section and has a transfer function with said zero.

9. (Currently Amended) A phase locked loop circuit as claimed in ~~any one of claims 3-5~~ claim 3, wherein said frequency divider device ~~(6)~~ is connected in series with a device ~~(71; 75)~~ having a transfer function with a zero.

10. (Currently Amended) A phase locked loop circuit as claimed in claim 9 wherein said device ~~(71; 75)~~ having a transfer function with a zero has an input connected to the controlled oscillator ~~(5)~~ and an output connected to an input ~~(61)~~ of the frequency divider ~~(6)~~.

11. (Currently Amended) A phase locked loop circuit as claimed in claim 9, wherein said device ~~(71; 75)~~ having a transfer function with a zero has an input connected to an output of the frequency divider ~~(6)~~ and an output connected to an input of the phase detector section

12. (Currently Amended) A phase locked loop circuit as claimed in claim 4 ~~claims 4 and 11~~, wherein said device ~~(74)~~ having a transfer function with a zero has a first input ~~(741)~~ connected to said delta-sigma modulator ~~(8)~~ and a second input ~~(742)~~ connected to the output of the frequency divider ~~(6)~~.

13. (Currently Amended) A phase locked loop circuit as claimed in claim 10, wherein said device ~~(71; 75)~~ having a transfer function with a zero comprises:

a device ~~(75)~~ with a transfer function equal to $\tau_s s$, said device with a transfer function equal to $\tau_s s$ with a device input ~~(751)~~ connected to the output of the oscillator ~~(4)~~,

said device ~~(71; 75)~~ having a transfer function with a zero further comprising:

a combiner device ~~(210)~~ with:

a first combiner input connected to the output of the device ~~(75)~~ with a transfer function equal to $\tau_s s$;

a second combiner input connected to the input of the device ~~(75)~~ with a transfer function equal to $\tau_s s$, and

a combiner output ~~(752)~~ connected to the input of the frequency divider device ~~(6)~~.

14. (Currently Amended) A method for generating a periodic signal, ~~at least comprising~~ comprising the steps of:

receiving a periodic signal of a first frequency;

comparing a phase of said periodic signal with a phase of a reference signal

generating a difference signal relating to a phase difference between said periodic signal and said reference signal;

filtering said difference signal;

generating an output signal with a frequency corresponding to an amplitude of said difference signal;

transmitting said output signal further;

generating said reference signal by changing said output signal such that the frequency of the output signal is lowered;

wherein for said changing of said output signal a feedback circuit having a transfer function with at least one zero, is used, and said receiving a periodic signal until said transmitting said output signal involves a closed loop transfer function without zeros.

15-16. (Cancelled)

17. (New) The method of Claim 14 wherein said feedback circuit includes at least one frequency divider device.

18. (New) The method of Claim 17 wherein said frequency divider device performs a transfer function with said zero.

19. (New) The method of Claim 17 wherein said feedback circuit includes a first frequency divider device and a second frequency divider device, said second frequency divider device performs a transfer function with a zero.